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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,020	12/31/2001	Sung H. Kuo	H052617.1131US0	7525

7590 07/14/2004

HEWLETT-PACKARD COMPANY  
INTELLECTUAL PROPERTY ADMINISTRATION  
P.O. BOX 272400  
FORT COLLINS, CO 80527-2400

EXAMINER

THAI, XUAN MARIAN

ART UNIT	PAPER NUMBER
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2111

DATE MAILED: 07/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/039,020	KUO, SUNG H.	
	<b>Examiner</b>	<b>Art Unit</b>	
	XUAN M. THAI	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 31 December 2001.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-28 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-28 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 31 December 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 12/31/01.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

**DETAILED ACTION**

1. This is in response to communication filed on December 31, 2001. Claims 1-28 are pending in the application.

***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Cepulis et al. (USPN 6,061,754; Cepulis).

As per claims 1 and 14, Cepulis discloses a computer system (e.g. figs. 2, 3, 4, 6 and 7), comprising: a processor (e.g. 101); a bridge (e.g. 208 or 209; col. 4, lines 40-43) coupled to the processor; a first expansion bus (e.g. 110 or 610) coupled to the bridge; a second expansion bus (e.g. 220 or 620) coupled to the bridge; a plurality of expansion slots (e.g. 331-336); and a bus switching mechanism (e.g. 451-454 or 631-636; col. 6, lines 10-50 and col. 7, lines 14-44) to assign at least one of the plurality of expansion slots between the first expansion bus and the second expansion bus (e.g. col. 6, lines 10-50 and col. 7, lines 14-44).

As per claim 2, “wherein the bus switching mechanism dynamically assigns at least one of the plurality of expansion slots based on a number of available expansion slots” is within the teachings of Cepulis. See e.g. col. 7, lines 39-44.

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As per claim 3, “wherein the bus switching mechanism dynamically assigns at least one of the plurality of expansion slots based on a type of a device in at least one of the plurality of expansion slots” is within the teachings of Cepulis. See e.g. col. 4, line 66 to col. 5, lines 36).

As per claim 4, “an expansion slot of the plurality of expansion slots, comprising: a presence detect pin to detect a type of a device in the expansion slot and to provide a bus selection signal to the bus switching mechanism to indicate a type of bus between the first expansion bus and the second expansion bus to connect with the expansion slot, the type of expansion bus matching the type of the device” is within the teachings of Cepulis in that Cepulis indicated that both software and hardware in the computer system can control the state of the switches (col. 7, lines 15-18).

As per claim 5, wherein the expansion slot fits a first device type and a second device type is within the teachings of Cepulis. See e.g. flexible connection points 434-436; col. 5, lines 46-47.

As per claim 6, Cepulis teaches “wherein the bus switching mechanism dynamically assigns at least one of the plurality of expansion slots based on a software programmable bus selection signal.” See col.7, lines 15-18.

As per claim 7, Cepulis teaches, “wherein the software programmable bus selection signal comprises a general purpose input/output signal.” See col.7, lines 15-18.

As per claim 8, Cepulis teaches “wherein the first expansion bus and the second expansion bus comprise buses of a different bit size.” See col. 1, lines 40-47.

As per claim 9, Cepulis teaches “wherein the first expansion bus and the second expansion bus comprise buses of a same bit size.” See col. 1, lines 40-47 and fig. 6.

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As per claim 10, Cepulis teaches “wherein the first expansion bus and the second expansion bus comprise buses of a different type.” See col. 8, lines 32-37.

As per claim 11, Cepulis teaches “wherein the first expansion bus and the second expansion bus comprise buses of a different speed.” See fig. 4.

As per claim 12, Cepulis teaches “wherein the first expansion bus and the second expansion bus comprise buses of a same type.” E.g. see figs. 3, 4 or 6.

As per claim 13, Cepulis teaches “wherein the first expansion bus and the second expansion bus comprise buses of a same speed.” See fig. 6.

As per claim 15, Cepulis teaches “wherein the bus switching mechanism comprises a multiplexor.” See col. 6, lines 28-30).

As per claim 16, Cepulis teaches a method of dynamic load balancing in a computer system including a plurality of expansion slots (e.g. 331-336) and a plurality of expansion buses (e.g. 110, 220 or 610 and 620), the plurality of expansion buses including a first expansion bus (e.g. 110 or 610) and a second expansion bus (e.g. 220 or 620), the method comprising the steps of: generating a bus selection signal; and switching electrical connection of an expansion slot of the plurality of expansion slots from the first expansion bus to the second expansion bus corresponding to the bus selection signal (col. 6, lines 10-50 and col. 7, lines 14-44).

As per claim 17, Cepulis teaches “wherein the bus selection signal is software Programmable” (col. 7, lines 15-18).

As per claim 18, Cepulis teaches “wherein the bus selection signal comprises a presence detect signal to detect a type of a device in the expansion slot.” (Col. 7, lines 15-18).

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As per claim 19, Cepulis teaches “wherein the bus selection signal comprises a presence detect signal to detect a bit size of a device in the expansion slot. (See col. 1, lines 40-47; Col. 7, lines 15-18 and fig. 6).

As per claim 20, “wherein the bus selection signal is based on a plurality of presence detect signals to detect availability of each expansion slot of the plurality of expansion slots” is within the teachings of Cepulis. See col. 5, lines 20-36 and col. 7, lines 15-18.

As per claim 21, “wherein the first expansion bus comprises a Peripheral Component Interconnect (PCI) bus” is disclosed by Cepulis. See Figs. 2, 3, 4, or 6.

As per claim 22, “wherein the bus selection signal is based on a load of the plurality of expansion buses” is within the teachings of Cepulis. See col. 5, lines 20-36 and col. 7, lines 15-18.

As per claim 23, “holding a plurality of devices in the plurality of expansion slots in a reset state until the switching step is complete” is within the teachings of Cepulis. Col. 7, lines 15-18.

As per claim 24, “isolating the first expansion bus from the expansion slot” is within the teachings of Cepulis. See col. 6, lines 32-51.

As per claim 25, “wherein the expansion slot comprises a Peripheral Component Interconnect (PCI) slot” is disclosed by Cepulis. See Figs. 2, 3, 4, or 6.

As per claim 26, “wherein the first expansion bus comprises a Peripheral Component Interconnect X (PCI-X) bus” is within the teachings of Cepulis. See col. 9, lines 10-11.

As per claim 27, “resetting the computer system after the switching step” is within the teachings of Cepulis. Col. 7, lines 15-18.

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As per claim 28, "wherein the bus selection signal comprises a presence detect signal to detect a speed of a device in the expansion slot" is disclosed by Cepulis. See col. 1, lines 40-47 and figs. 4 and 6.

***Conclusion***

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See attached Form PTO-892.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to XUAN M. THAI whose telephone number is 703-308-2064. The examiner can normally be reached on Monday to Friday from 8:30 A.M. to 5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



XUAN M. THAI  
Primary Examiner  
Art Unit 2111

XMT